METHOD OF BUILDING A CMOS STRUCTURE ON THIN SOI WITH SOURCE/DRAIN ELECTRODES FORMED BY IN SITU DOPED SELECTIVE AMORPHOUS SILICON

ABSTRACT

The present invention provides improved controllability of the lateral etch encroachment of silicon under the spacer, in light of the fact that the exemplary method, in accordance with the present invention, comprises the step of implanting neutral ions such as Ge or Ar into the source/drain regions. The implantation creates an amorphous silicon surface, and leaves a laterally extended amorphous layer under the spacer and a well defined amorphous/crystalline interface. The etch of silicon then extends laterally underneath the spacer, due to the higher etch rate of amorphous silicon and abrupt interface between amorphous and crystalline silicon.